VLSI Implementation of Very High SpeedLDPC Decoder

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***Abstract* -** **This paper presents high-throughput decoder architecture for generic quasi-cyclic low-density parity-check (QC-LDPC) codes. Various optimizations are employed to increase the clock speed. A row permutation scheme is proposed to significantly simplify the implementation of the shuffle network in LDPC decoder. An approximate layered decoding approach is explored to reduce the critical path of the layered LDPC decoder.**

Keywords – VLSI, LDPC, Decoder, Permutation, Parity Check

1. INTRODUCTION

Due to their near Shannon limit performance and inherently parallelizable decoding scheme; low-density parity-check (LDPC) codes have been extensively investigated in research and practical applications. Recently, LDPC codes have been considered for many industrial standards of next generation communication systems such as DVB-S2, WLAN (802.11.n), WiMAX (802.16e), and 10GBaseT (802.3an).

For high throughput applications, the decoding parallelism is usually very high. Hence, a complex interconnect network is required which consumes a significant   amount of silicon area and power. In a pioneering design of high throughput LDPC decoder, the utilization of chip area was only 50%.

In practice, QC-LDPC codes have attracted considerable attention due to their excellent error correction performance and the regularity in their parity check matrices which is well suited for VLSI implementation.

In this paper, we present a high-throughput low-cost layered decoding architecture for generic QC-LDPC codes. A row permutation approach is proposed to significantly reduce the implementation complexity of shuffle network in the LDPC decoder. An approximate layered decoding approach is explored to increase clock speed and hence to increase the decoding throughput. An efficient implementation technique which is based on Min-Sum algorithm is employed to minimize the hardware complexity. The computation core is further optimized to reduce the computation delay.

2. OVERALL DECODER ARCHITECTURE

The proposed decoder computes the check-to-variable messages, variable-to-check messages, and LLR messages corresponding to an entire block row of Hp matrix in one clock cycle. The decoder architecture is shown in Figure. It consists of the following five portions.

1) L layer R register arrays. Each layer is used to store the check-to variable messages Rcv corresponding to the 1-components in a block row of matrix Hp. At each clock cycle, Rcv messages in one layer are vertically shifted down to the adjacent layer.
2) A check node unit (CNU) array for generating the Rcv messages for one layer of R-register array in a clock cycle. The dashed-lines in the CNU array denote two pipeline stages.
3) C LLR-register arrays. Each LLR-register array stores the Lv messages corresponding to a block column of matrix Hp   .
4) C variable node unit (VNU) arrays. Each VNU array is used for computing the variable-to-check messages and LLR messages corresponding to a block column of matrix Hp . Each VNU is composed of two adders.
5) C data shifters. The Lv messages corresponding to a block column of matrix Hp is shifted one step by a data shifter array.
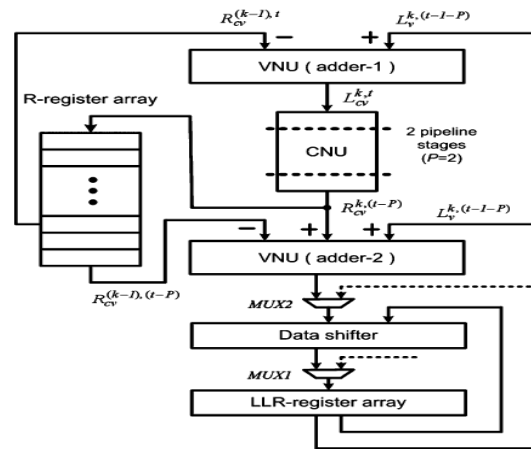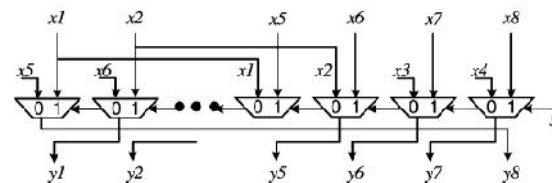

Figure 1. Block Diagram

Figure 2.Data Shifter

Figure shows the structure of a data shifter for the matrix Hp. When the value of control signal S is 1, the

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shifting network performs a single-step left cyclic-shift. If S is set to 0, the reverse cyclic-shift is performed.
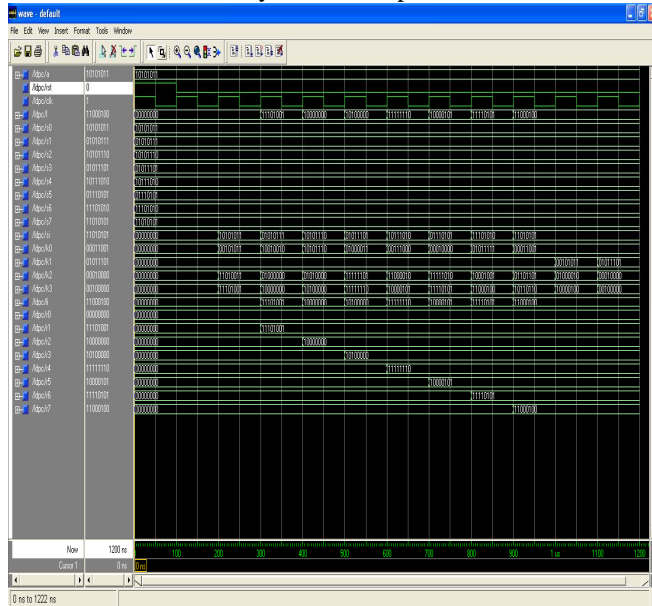

Figure 3. Output Waveform

3. CONCLUSION

In this paper, high-throughput low-complexity decoder architecture for generic QC-LDPC codes has been presented. To enable pipelining technique for layered decoding approach, an approximate layered decoding approach has been explored. QC-LDPC code constructed using PEG approach is used to demonstrate the decoding performance and estimate the decoding throughput and hardware cost.

4. REFERENCES

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